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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/463,900	04/03/2000	HANS GUDE GUDESEN	2834-119P	6936

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/463,900	GUDESEN ET AL	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 July 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *17-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *17-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *03 April 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s) _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

The drawings are objected to for the following reasons.

Figure 1 is not designated by a legend such as "Prior Art". The Legend is necessary in order to clarify what applicant's invention is (see MPEP § 608.02g).

Applicant is required to submit a proposed drawing correction, showing changes in red ink, in response to this Office action. However, formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner (see MPEP § 608.02v).

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17-32 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,793,115 to Zavracky et al.

Regarding to claim 17, Zavracky discloses a scaleable integrated data processing device, provided on a carrier substrate 220, comprising a processing unit having one or more processors 100, 200, and a storage unit having one or more memories 210, 108,

wherein the data processing device comprises mutually adjacent, substantially parallel stacked layers (P.M.MP) (fig. 13) and the processing unit and the storage unit are provided in one or more of the substantially parallel stacked layers, wherein each of the substantially parallel stacked layers comprises one or more processors and/or one or more memories, and electrical conducting structures 114, 224, 140 which form internal electrical connections in the layer, wherein each substantially parallel stacked layer is formed of a plurality of sublayers, having delimited portions which form dielectric, semiconducting or electrical conducting areas in the sublayer and the sublayer, in addition to at least one dielectric portion, having one or more semiconducting and/or electrical conducting portions, wherein delimited portions with a given electrical property in each sublayer are provided in a registering relationship to one or more corresponding portions in at least one of the adjacent neighbour sublayers to form integrated circuit elements which extend vertically through one or more sublayers, wherein the electrical conducting structures are formed by the electrical conducting portions in the sublayer and respectively extend horizontally in order to create horizontal electrical conducting structures or are provided in registering connection with corresponding electrical conducting portions in one or more adjacent sublayers, such that the electrical conducting structures integrated in the sublayers form three-dimensional electrical interconnecting networks in the layers and interconnect the circuit elements therein mutually in three dimensions, and wherein additional electrical conducting structures in the data-processing device interconnect the layers mutually and/or the layers with the substrate and in order

to create a connection to the exterior of the data processing device as set forth in col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1.

Regarding to claim 18, a scaleable integrated data processing device according to claim 17, wherein the sublayers in one or more of the substantially parallel stacked layers are realized in a technology which on a first level of a functional hierarchy configures functionally one or more of the layers as a combined processor and memory layer (MP), or one or more the layers substantially as processor layers (P) or one or more the layers substantially as memory layers (M) (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 19, a scaleable integrated data processing device, wherein the processing unit in a layer (P, MP) is configured functionally on a second level of the functional hierarchy as one or more processors or parts of one or more processors, at least one processor constituting a central processing unit or microprocessor in the data processing device, and possible further processors optionally being configured as control and/or communication processors respectively (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 20, a scaleable integrated data processing device, wherein the central processing unit is configured functionally on a third level of the functional hierarchy as a parallel processor with several execution units working in parallel provided

in one and the same layer (P, MP) or in two or more layers (P, MP) or in sublayers thereof to provide an optimal interconnection topology (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 21, a scaleable integrated data processing device, wherein more than one central processing unit is provided, wherein each central processing unit is mutually interconnected and adapted for working in parallel and provided in one and the same layer (P, MP) or in two or more layers (P, MP) to provide an optimal interconnection topology (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 22, a scaleable integrated data processing device, wherein the storage unit in a layer (M,MP) is configured functionally on the second level of the functional hierarchy as one or more memories or parts of one or more memories, at least one memory constituting a RAM and being connected with at least one control processing unit or microprocessor, and possible further memories optionally being configured as high-speed memories, ROMs, WORM, ERASABLE and REWRITEABLE respectively (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 13).

Regarding to claim 23, a scaleable integrated data processing device, wherein two or more RAMs are connected to a central processing unit and respectively assigned to two or more subunits in the central processing unit, RAMs and the subunits being

distributed in selected combinations in one or more layers (P, M, MP) to provide an optimal interconnection topology (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 13).

Regarding to claim 24, a scaleable integrated data processing device, wherein two or more central processing units are provided which are connected with one or more common RAM or RAMs, and each central processing unit is provided in mutually adjacent layers (P, MP), or distributed in selected combinations between two or more layers (P, MP), and that the common RAM or RAMs are provided in selected combinations in one or more of the layers (P, MP) and/or in one or more memory layers (M) adjacent to the latter or interfoliated there between to provide an optimal interconnection topology (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 13).

Regarding to claim 25, a scaleable integrated data processing device, wherein at least a part of the storage unit constitutes a mass memory, the mass memory optionally being configured as RAM, ROM, WORM, ERASABLE or REWRITEABLE or combinations thereof (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 13).

Regarding to claim 26, a scaleable integrated data processing device, wherein the data processing unit comprises several processor layers (P) and several memory layers (M), and the memory layers (M), in order to reduce the signal paths there between and

the processor layers (P), are interfoliated between the latter (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 27, a scaleable integrated data processing device, wherein further electrical structures are provided as electrical edge connections on or over at least one side edge of one or more layers (P,M,MP) in order to contact electrical conducting structures in other layers and/or provide electrical connection between layers and substrate (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 28, a scaleable integrated data processing device, wherein the further electrical conducting structures are provided as vertical conducting structures in one or more layers (P, M, MP) and form electrical connections in the cross-direction of the layers and perpendicular to their planes in order to contact electrical conducting structures in other layers and/or to provide electrical connection between the layers and substrate (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 29, a scaleable integrated data processing device, wherein one or more layers (P, M, MP) are formed of an organic thin-film material, the organic thin-film material or materials selected from the group consisting of monomeric, oligomeric and polymeric organic materials and metal-organic complexes, and combinations thereof (cols. 5-15).

Regarding to claim 30, a scaleable integrated data processing device , wherein all layers (P, M, MP) are formed of organic thin-film material (cols. 5-15).

Regarding to claim 31, a scaleable integrated data processing device, wherein one or more layers (P, M, MP) are formed of inorganic thin-film material, the inorganic thin-film material or materials being selected from the group consisting of crystalline, polycrystalline and amorphous thin-film materials, and combinations thereof (cols. 5-15).

Regarding to claim 32, a scaleable integrated data processing device according to claim 17, wherein two or more layers (P, M, MP) are formed of both organic and inorganic thin-film materials or combinations thereof, the organic thin-film material or materials being selected from the group consisting of monomeric, oligomeric and polymeric organic materials and metal-organic complexes, and combinations thereof, and the inorganic thin-film material or materials being selected from the group consisting of crystalline, polycrystalline and amorphous thin-film materials, and combinations thereof (cols. 5-15).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran. (703) 305-1958. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mai-Huong Tran

HOAI HO
PRIMARY EXAMINER